CChu_Job_1_of_1

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Document Listing

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US006282095	10	1 - 10
US006075700	10	1 - 10
US005621615	17	1 - 17
JP403196657A	4	1 - 4
Total (4)	41	-

6353265 — 102 (6) Fig. 11

claim 5 — 6337521 — 102?

6297547 ≡ 6175149

6153928

6133069

5793101 ≡ 5719436

5596225

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2346711

supporting the semiconductor chips, and a base support plate separated from said heat sink plate by an insulating plate, wherein said semiconductor chips, said internal heat sink plate, said insulating plate and said base support plate are all bonded together by solder or metal brazing material, wherein the thickness of the base support plate is more than 2.5 times in maximum thickness of the internal support plate, wherein by forming plating layers on and beneath said insulating plate with the insertion of metallization patterns on either sides of the insulating plate, and bonding heat sink plates respectively to the upper and lower plating layers with the insertion of solder layers over the plating layers, the areas of said plating layers are made smaller than the areas of said heat sink plates disposed on and beneath said plating layers.

4. A semiconductor module including a plurality of semiconductor chips, an internal heat sink plate for supporting the semiconductor chips, and a base support plate separated from said heat sink plate by an insulating plate, wherein said semiconductor chips, said internal heat sink plate, said insulating plate and said base support plate are all bonded together by solder or metal brazing material, wherein the thickness of the base support plate is more than 2.5 times in maximum thickness of the internal support plate, wherein Mo heat sink plates are disposed beneath the semiconductor chips, wherein said internal heat sink plate comprises a Cu heat sink plate disposed beneath said Mo heat sink plates, and wherein an Mo heat sink plate is disposed on a side of said Cu heat sink plate which faces toward said base support plate.

5. A semiconductor module including a plurality of semiconductor chips, an internal heat sink plate for supporting the semiconductor chips, and a base support plate separated from said heat sink plate by an insulating plate, wherein said semiconductor chips, said internal heat sink plate, said insulating plate and said base support plate are all bonded together by solder or metal brazing material, wherein the thickness of the base support plate is more than 2.5 times in maximum thickness of the internal support plate, wherein when the area of the base support plate is 40 cm^2 or more, the thickness of said base support plate is 8 mm or more.

6. A semiconductor module including a plurality of semiconductor chips, an internal heat sink plate for supporting the semiconductor chips, and a base support plate separated from said heat sink plate by an insulating plate, wherein said semiconductor chips, said internal heat sink plate, said insulating plate and said base support plate are all bonded together by solder or metal brazing material, wherein the thickness of the base support plate is more than 2.5 times in maximum thickness of the internal support plate, wherein when a plurality of said semiconductor chips are bonded to said internal heat sink plate and a plurality of electrodes are wired between the semiconductor chips on the internal heat sink plate, a predetermined insulation distance between the terminals of the device is set in the through-thickness direction of said insulating plate disposed beneath the wires or the electrodes.

7. A semiconductor module, comprising:

a base support plate;

an insulating plate bonded on the base support plate;

a first heat sink plate bonded on the insulating plate;

a plurality of second heat sink plates bonded on the first heat sink plate; and

a plurality of semiconductor chips bonded on the plurality of second heat sink plates, wherein

a thickness of the base support plate is equal to 2.5 times or greater than that of the first heat sink plate and the thickness of the first heat sink plate is equal to 2.0 times or greater than that of at least one of the second heat sink plates.

8. A semiconductor module according to claim 7, wherein the first heat sink plate is comprised of copper and at least one of the second heat sink plates is comprised of molybdenum.

9. A semiconductor module according to claim 7, wherein the base support plate and the insulating plate, the insulating plate and the first heat sink plate, the first heat sink plate and the plurality of second heat sink plate, and the plurality of second heat sink plate and the plurality of semiconductor chips are respectively bonded together by one of solder and metal brazing material.

10. A semiconductor module according to claim 8, wherein the base support plate and the insulating plate, the insulating plate and the first heat sink plate, the first heat sink plate and the plurality of second heat sink plates, and the plurality of second heat sink plates and the plurality of semiconductor chips are respectively bonded together by one of solder and metal brazing material.

11. A semiconductor module according to claim 7, wherein a thickness of one of a solder and a metal brazing material around a peripheral portion of the insulating plate where the base support plate and the insulating plate are bonded as well as the insulating plate and the first heat sink plate, is equal to or greater than that of a middle portion of the insulating plate.

12. A semiconductor module according to claim 10, wherein a thickness of one of the solder and metal brazing material around a peripheral portion of the insulating plate where the base support plate and the insulating plate are bonded as well as the insulating plate and the first heat sink plate, is equal to or greater than that of a middle portion of the insulating plate.

13. A semiconductor module according to claim 9, wherein a thickness of one of the solder and metal brazing material around a peripheral portion of the insulating plate where the base support plate and the insulating plate are bonded as well as the insulating plate and the first heat sink plate, is equal to 1.5 times or greater than that of a middle portion of the insulating plate.

14. A semiconductor module according to claim 10, wherein a thickness of one of the solder and metal brazing material around a peripheral portion of the insulating plate where the base support plate and the insulating plate are bonded as well as the insulating plate and the first heat sink plate, is equal to 1.5 times or greater than that of a middle portion of the insulating plate.

15. A semiconductor module according to claim 9, further comprising: a metallizing layer formed on the insulating plate; and a plating layer formed on the insulating plate through the metallizing layer and having a smaller area than that of the first heat sink plate.

16. A semiconductor module according to claim 10, further comprising: a metallizing layer formed on the insulating plate; and a plating layer formed on the insulating plate through the metallizing layer and having a smaller area than that of the first heat sink plate.

17. A semiconductor module according to claim 7, further comprising a third heat sink plate located between the insulating plate and the first heat sink plate.

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Document Listing

Document	Selected Pages	Page Range
US005923052	7	1 - 7
Total (1)	7	-

	Document ID	Issue Date	Current OR	Inventor
1	US 6353265 B1	20020305	257/777	Michii, Kazunari
2	US 6344687 B1	20020205	257/724	Huang, Chih-Kung et al.
3	US 6313527 B1	20011106	257/723	Han, Charlie et al.
4	US 6175149 B1	20010116	257/676	Akram, Salman
5	US 6133067 A	20001017	438/110	Jeng, Jacob et al.
6	US 5793108 A	19980811	257/723	Nakanishi, Hiroyuki et al.
7	US 5719436 A	19980217	257/676	Kuhn, Harry A.
8	US 5625226 A	19970429	257/705	Kinzer, Daniel M.
9	US 5596225 A	19970121	257/667	Mathew, Ranjan J. et al.
10	US 5147815 A	19920915	29/827	Casto, James J.
11	JP 11317488 A	19991116		INABA, TAKEHITO et al.
12	JP 10256470 A	19980925		TSUBONOYA, MAKOTO

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Summary

Document	Pages	Printed	Missed
US006258618	9	9	0
US005917202	8	8	0
US005416342	15	15	0
Total (3)	32	32	0

4. The device of claim 3, which further includes a second adhesive for connecting the one surface of the second die to the second surface of the pad.

5. The device of claim 4, wherein the second adhesive is electrically insulative.

6. The device of claim 3, wherein selected ones of the plurality of electrodes are connected to selected ones of the plurality of pins within the insulation housing

7. The device of claim 4, wherein selected ones of the plurality of electrodes are connected to selected ones of the plurality of pins within the insulation housing.

8. The device of claim 5, wherein selected ones of the plurality of electrodes are connected to selected ones of the plurality of pins within the insulation housing.

9. The package of claim 2, wherein the first and second die are MOSgated power devices; and wherein the first surfaces of the first and second die each contain a power electrode to be connected to the pad section and to one another. → no fig.

10. The package of claim 9, wherein the first and second die are fixed to the pad section by a conductive adhesive.

11. The package of claim 2, wherein the first die is a MOSgated power device and the second die is a control IC coupled to selected electrodes of the first die.

no. fig.

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US005917202	8	1 - 8
US005416342	15	1 - 15
Total (3)	32	-

DETAILED ACTION

1. a semiconductor device package comprising

- a lead frame having a conductive pad section with first and second opposite surfaces and
- a plurality a coplanar pin sections,
- a first and at least a second semiconductor die, each having first and second opposite surfaces and each having a plurality of electrodes;
- the first electrodes of each of the first and second die being fixed to and in surface to surface connection with the first and second opposite surfaces respectively of the pad section; 112 2nd
- the first and second die being in spatial overlapping relationship with respect to one another; and Spatial?
- an insulation housing enclosing the die and the pad section;
- the pin section extending through the surface of the insulation housing to its exterior.

2. The device of claim 1, wherein selected ones of the plurality of electrodes are connected to selected ones of the plurality of pins within the insulation housing.

3. The device of claim 1, which further includes a conductive adhesive for connecting the one surface of the first die to the first surface of the pad.

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US005850102	12	1 - 12
Total (1)	12	-

Mark Pavier

F. D. : 1/15/02

E. F. D. : 1/19/01

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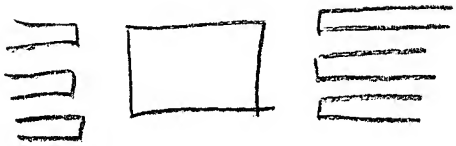
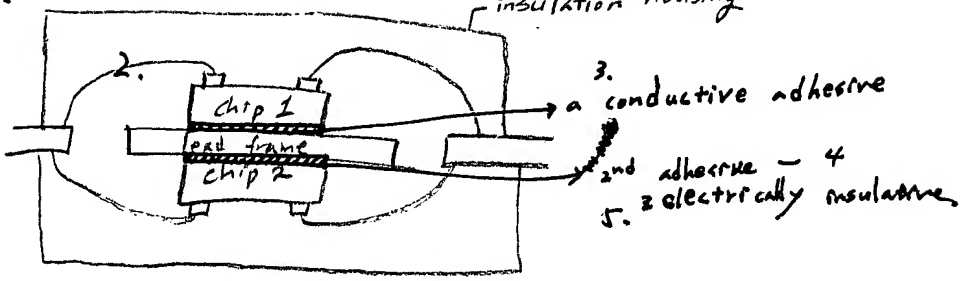
lead frame

1.





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171 783
676 ? 787
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685 ?
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458 / 108 → 109

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Document Listing

Document	Selected Pages	Page Range
US005376584	8	1 - 8
Total (1)	8	-

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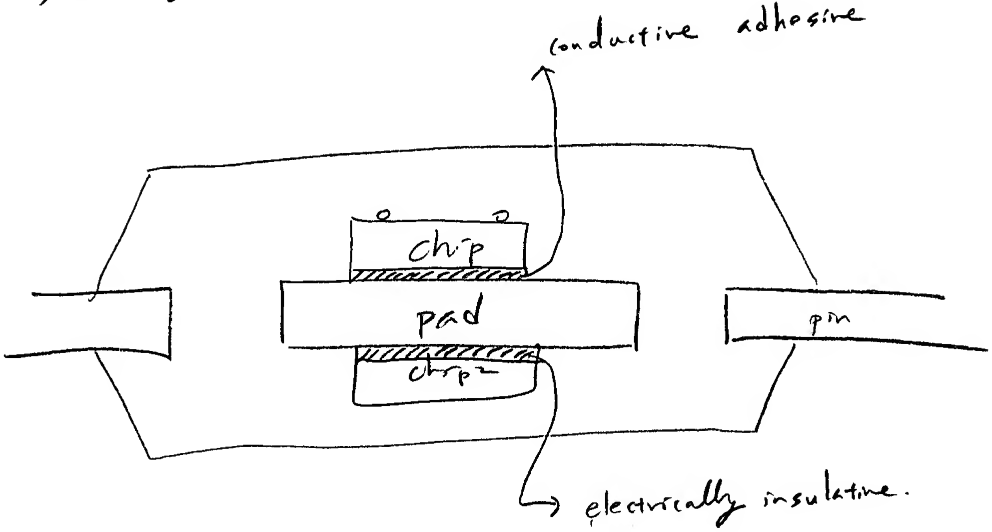

Q [2 [4 9-10
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